

<b>Notice of References Cited</b>	Application/Control No. 09/883,922	Applicant(s)/Patent Under Reexamination ONO ET AL.	
	Examiner Matthew A. Anderson	Art Unit 1765	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-4981549	01-1991	Ichiro et al.	C30B 15/00
	B	US-5817171	10-1998	Sakurada et al.	117/13
	C	US-6120598	09-2000	Iida et al.	117/13
	D	US-6179911 B1	01-2001	Tomioka et al.	117/20
	E	US-5935320	08-1999	Graef et al.	117/2
	F	US-6077343	06-2000	Iida et al.	117/2
	G	US-6261361 B1	07-2001	Iida et al.	117/19
	H	US-6045610	04-2000	Park et al.	117/13
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	EP0962557	12-1999	EPO	Iida et al.	C30B 15/00
	O	EP0909840	04-1999	EPO	Iida et al.	C30B 15/00
	P	EP0747513 A2	12-1996	EPO	Takano et al.	C30B 15/00
	Q	EP0716168 A1	06-1996	EPO	Takano et al.	C30B 15/00
	R	EP0890662	01-1999	EPO	Iida et al.	C30B 15/00
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf et al., Silicon Processing for the VLSI Era, Volume 1: Process Technology, Lattice Press, Sunset Beach, CA, USA, pp. 8-11, 27-33, 36-72, 124, 139-142, 1986.
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.